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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,236	03/26/2001	Masashi Asakawa	100021-00046	8733

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EXAMINER

CHOI, WOO H

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 04/06/2004

16

Please find below and/or attached an Office communication concerning this application or proceeding.

OR

Office Action Summary

Application No.

09/816,236

Applicant(s)

ASAKAWA ET AL.

Examiner

Woo H. Choi

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☒ Claim(s) 1 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Claim Objections

1. Claim 1 recites the limitations “said storage unit” and “said logical memory unit” in line 7. Applicant seems to be regarding “storage units” and “logical memory units” recited prior to the limitations as the antecedent bases. However, the plural versions of the limitations are not proper antecedent bases. Applicant should provide proper antecedent bases for these limitations, for example, by adding a limitation such as “wherein each storage unit corresponds to a logical memory unit” or other similar limitations.

Claim 1 also recites the limitation “said memory block” in line 11. This limitation should be changed to “said logical memory block”.

Appropriate action is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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3. Claims 1 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama *et al.* (US Patent No. 5,574,876, hereinafter “Uchiyama”) in view of Fadavi-Ardekani *et al.* (US Patent No. 6,401,176, hereinafter Fadavi-Ardekani”).

4. With respect to claim 1, Uchiyama discloses a synchronous DRAM comprising:

one memory array divided into a plurality of logical memory blocks (Figure 1 102, see also Figure 4, MS area is divided into logical blocks that correspond to banks);

mode storage units so disposed in a plurality of stages as to correspond to said memory blocks, for storing control information for defining operation modes of said logical memory blocks (Figure 4, Figure 5A, 505 and col. 5, lines 50 – 64. MS 102 is comprised of 4 chips shown in figure 5A and is organized as logical blocks as shown in figure 4);

a setting unit for setting the control information designated by a mode setting instruction to said mode storage unit corresponding to said memory block designated by said mode setting instruction in accordance with said mode setting instruction outputted from a controller (col. 5, lines 60 – 64);

a mode selection unit for selecting said mode storage unit corresponding to said memory block containing a memory cell designated by an address inputted from one of the controllers (col. 7, lines 3 – 20); and

an access unit for executing an access operation in synchronism with a predetermined clock signal for the corresponding one of said logical memory blocks in accordance with the control information stored in said mode storage unit selected (This is inherent in any functional

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memory device, since storage of information for access is the main function of a memory device. Clock is shown in figure 6).

However, Uchiyama does not specifically disclose that mode setting instructions are outputted from a plurality of controllers. On the other hand, Fadavi-Ardekani discloses multiple controllers accessing a shared synchronous memory. It would have been obvious to one of ordinary skill in the art, having the teachings of Uchiyama and Fadavi-Ardekani before him at the time the invention was made, to use the multi-processor accessible shared synchronous memory teachings of the synchronous memory of Fadavi-Ardekani in the synchronous memory of Uchiyama, in order to allow for a more efficient use of memory resources in a multi-processor environment (Fadavi-Ardekani, col. 2, lines 35 – 43).

5. With respect to claim 2, said plurality of logical memory blocks is constituted by continuous memory cells designated by addresses (Uchiyama, Figure 4).

6. With respect to claim 3, wherein said plurality of logical memory blocks coincides with memory banks (Figures 4 and 5, memory banks 0 and 1).

7. With respect to claim 4, said setting unit includes an object selection unit for selecting said mode storage unit corresponding to a bit train on the basis of said bit train in the data outputted as a part of said mode setting instruction from a plurality of controllers, and setting it as a setting object of the control information (col. 7, lines 3 – 20, and col. 5, lines 58 – 64).

8. With respect to claim 5, said bit train is a bit train contained in the address outputted to an address bus (col. 7, lines 4 – 9).

9. With respect to claims 6, 7, and 8, wherein said bit train contained in said address is a bit train assigned to a test mode, a burst length, and CAS latency, respectively, merely recite nonfunctional description of contents of the bit train and do not patentably distinguish from their parent claim. To make them patentably distinct from the parent claims, claims should have functional utilities rather than mere assignment of labels. As currently claimed they do not claim different modes of operation of the memory. Positively claiming the different modes of operation would make them distinct from their parent claims.

10. With respect to claim 9, said bit train is a bit train contained in the data outputted to said data bus (col. 7, lines col. 10 – 13).

11. With respect to claim 10, said setting unit includes an input unit for inputting the control information to said mode storage unit as a setting object on the basis of the bit train outputted as a part of the mode setting instruction by said plurality of controllers to said address bus (col. 7, lines 3 – 20, and col. 5, lines 58 – 64, see also figures 5 and 7).

12. With respect to claim 11, said mode selection unit includes:

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a selector for acquiring information designating said logical memory blocks and selecting the control data outputted from the corresponding one of said mode register sets; and

an address generation unit for generating a series of addresses in accordance with the operation mode inputted (Figure 7, 704 and col. 7, lines 3 – 20).

13. With respect to claim 12, said access unit includes:

an address decoder for decoding an address input and designating the memory cell; and
an input/output control circuit for executing an access processing corresponding to the operation mode designated for the designated memory cell (figure 7, 104).

14. Rejections of claims 1 – 2 and 4 – 12 under 35 U.S.C. 103(a) based on the combined teachings of Usami and Fadavi-Ardekani detailed in the last Office Action mailed February 03, 2003, paper number 7, are maintained.

For the sake of clarity and brevity these rejection are not repeated here. Please refer to the Office Action mentioned above.

15. Rejection of claims 1 – 12 under 35 U.S.C. 103(a) based on the combined teachings of Rao and Usami detailed in the last Office Action are maintained.

16. Rejection of claims 1 – 12 under 35 U.S.C. 103(a) based on the combined teachings of Farrer and Fadavi-Ardekani detailed in the last Office Action are maintained.

Response to Arguments

17. Applicant seems to be arguing that there is a one-to-one correspondence between a mode storage unit and a logical memory block and that this allows each block to independently operate in different modes of operations. However, the independent claim does not properly establish one-to-one correspondence between a mode storage unit and a memory block. Neither does it recite independent operation of logical memory blocks in different modes in a shared environment. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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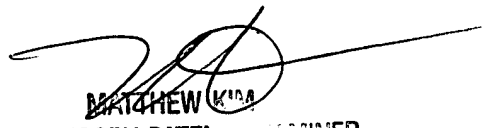
however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

whc
whc
October 20, 2003


MATTHEW KIM
SUPERVISORY PATER.
TECHNOLOGY CE